GigaDevice Semiconductor Inc.

GD32E23x Hardware Development Guide

Application Note
AN074

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Table of Contents

List of Figures

List of Tables

1. Introduction

This article is specially provided for developers of 32-bit general-purpose MCU GD32E23x series based on ARM® Cortex®-M23 architecture. It provides an overall introduction to the hardware development of GD32E23x series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this development guide is to allow developers to quickly get started and use GD32E23x series products, and quickly develop and use product hardware, save time for manual study, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32E23x series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32E23x series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32E23x series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32E23x series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32E23x series.
6. Reference circuit and PCB Layout design, mainly introduce GD32E23x series hardware circuit design and PCB Layout design considerations.
7. Package description, mainly introduces the package forms and names included in the GD32E23x series.

This document also satisfies the minimum system hardware resources used in application development based on GD32E23x series products.

Table 1-1. Applicable Products

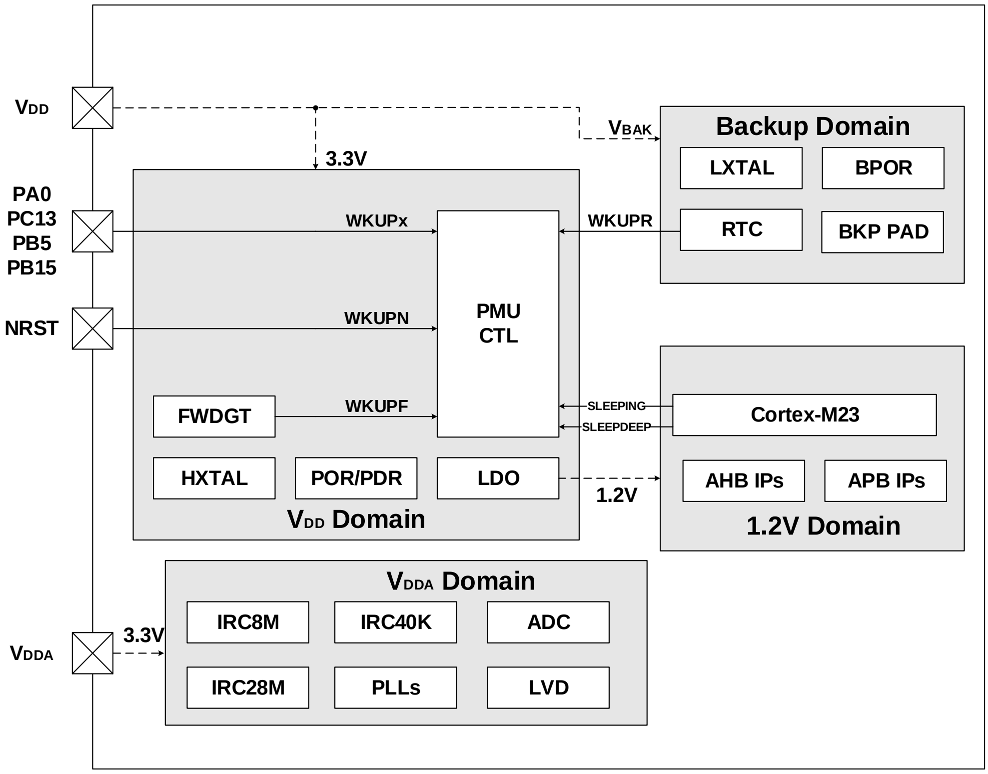
Type	Part Numbers
MCU	GD32E230xx series
	GD32E232xx series
	GD32E235xx series

2. Hardware Design

2.1. Power

The V_{DD}/V_{DDA} operating voltage range of GD32E23x series products is 1.8 V ~ 3.6 V. For GD32E23x series, there are three power domains, including V_{DD}/V_{DDA} domain, 1.2 V domain and backup domain, as is shown in ***Figure 2-1. GD32E23x Power supply overview***. The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2 V domain. The backup domain is powered directly by V_{DD}, and when the V_{DD} power is turned off, the backup domain power is lost.

Figure 2-1. GD32E23x Power supply overview



LVD: Low Voltage Detector
POR: Power On Reset
LDO: Voltage Regulator
PDR: Power Down Reset
BPOR: VBAK Power On Reset

2.1.1. Backup domain

The backup domain supply voltage range is 1.8 V ~ 3.6 V. In order to ensure the normal operation of the backup registers and RTC, the V_{DD} power cannot be turned off. Once the V_{DD} power is turned off, all backup domain data and registers will be reset.

Note: GD32E23x Series MCUs has no VBAT pin and cannot use RTC or backup domain to work normally after power failure.

2.1.2. V_{DD}/V_{DDA} domain

The V_{DD}/V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two should not exceed 300mV (the internal VDDA and VDD of the chip are connected through a back-to-back diode). To avoid noise, VDDA can be connected to VDD through an external filter circuit, and the corresponding VSSA is connected to VSS through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. The GD32E232xx internally integrates a VREF pin for independent power supply of the ADC (external power supply: 2.4 V≤V_{REF}≤V_{DDA}).

- V_{DD} power supply range: 1.8 V≤V_{DD}≤3.6 V.
- If the ADC function is not used, the V_{DDA} power supply range (1.8 V≤V_{DD}≤3.6 V); if the ADC function is used, the V_{DDA} power supply range (2.4 V≤V_{DD}≤3.6 V).

Note: GD32E232xx series have V_{REF} pins, which can be generated internally or provided externally.

2.1.3. V_{REF} domain

In order to improve the performance of ADC/DAC, a precise internal voltage reference circuit is integrated in the GD32E232xx series chip, which provides accurate reference voltage for ADC/DAC, and can also supply VREF pin through external power supply. The typical value of V_{REF} is generated internally: 2.5V, and the output can be enabled by the VREF_EN bit in the SYSCFG_CFG2 register. If the VREF_EN bit is not turned on, V_{REF} can be powered by an external power supply or connect to VDDA. At this time, the VREF_EN bit in the SYSCFG_CFG2 register must remain 0.

It is recommended to connect a 10nF+1uF ceramic capacitor to the ground outside the V_{REF} pin. If conditions do not allow, at least one 0.1uF ceramic capacitor should be connected to the ground.

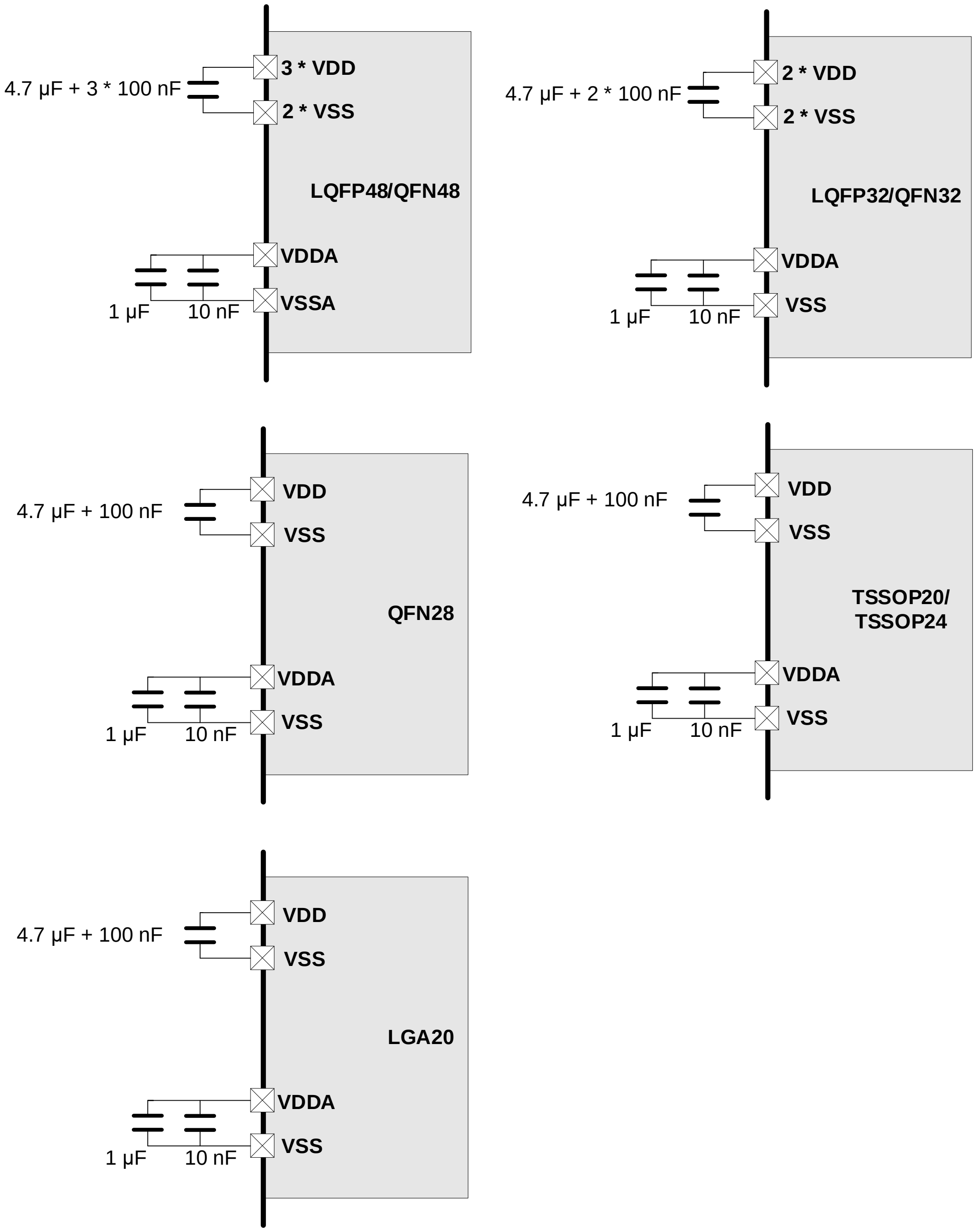
2.1.4. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF+1uF ceramic capacitor is recommended).
- V_{REF} of the GD32E232xx series can be generated internally or directly connected to

VDDA. For the GD32E230xx and GD32E235xx series, the VREF pin can only be directly connected to VDDA. A 10nF + 1uF ceramic capacitor should be connected from the VREF pin to ground.

Figure 2-2. GD32E230xx / GD32E235xx Recommended Power Supply Design

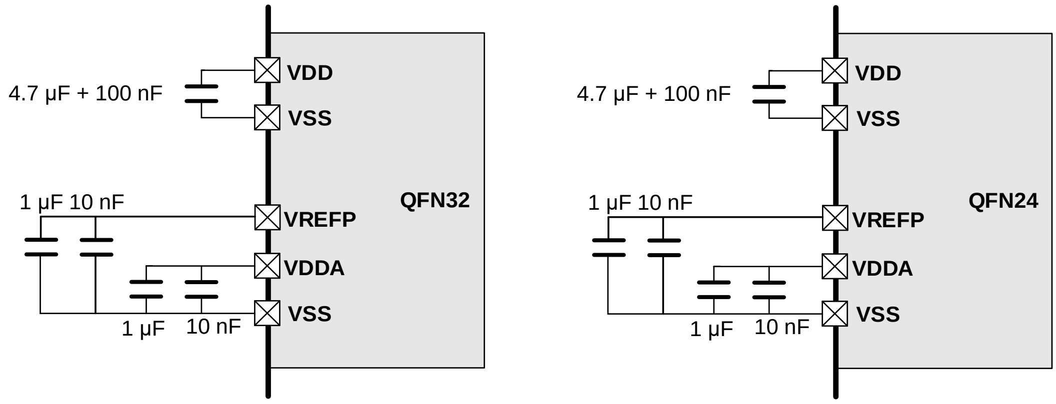


Note:

1. All decoupling capacitors must be placed close to the corresponding VDD, VDDA pins of the chip.
2. The recommended VREF selection is generated internally, and can also be provided externally according to the actual application of the customer.
3. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.

4. LQFP48/QFN48: VDDA, VREFP internal direct connection, VSSA, VREFN internal direct connection;
5. LQFP32/QFN32: Internal direct connection of VDDA and VREFP, and internal direct connection of VSS, VSSA and VREFN.
6. QFN28: VDDA and VREFP are directly connected internally, and VSS, VSSA and VREFN are directly connected internally.
7. TSSOP20: VDDA and VREFP are directly connected internally, and VSS, VSSA and VREFN are directly connected internally.
8. LGA20: VDDA and VREFP are directly connected internally, while VSS, VSSA and VREFN are directly connected internally.

Figure 2-3. GD32E232xx Recommended Power Supply Design



1. All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VREF pins of the chip.
2. The recommended VREF selection is generated internally, and can also be provided externally according to the actual application of the customer.
3. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
4. QFN32: VSS, VSSA and VREFN are directly connected inside.
5. QFN24: VSS, VSSA and VREFN are directly connected inside.

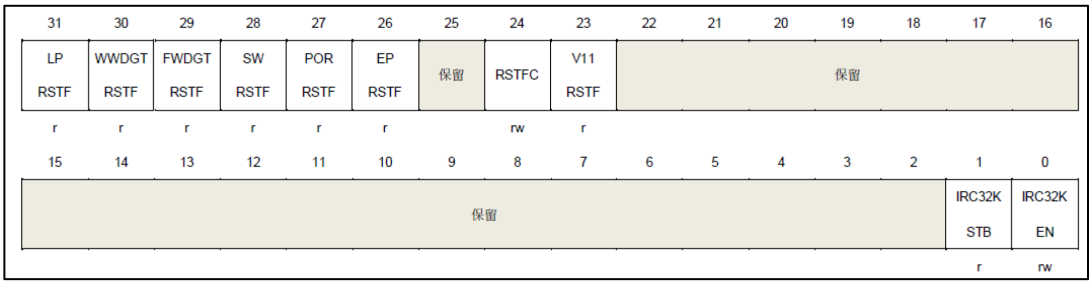
2.2. Power supply detection and reset

In this section, the default VDD and VDDA pins remain connected and are powered by the same power supply.

GD32E23x series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on. During the power and system reset process, NRST will maintain a low level until the reset is over. When the MCU cannot be executed, the NRST pin waveform can be monitored by an oscilloscope to determine whether the chip has been reset.

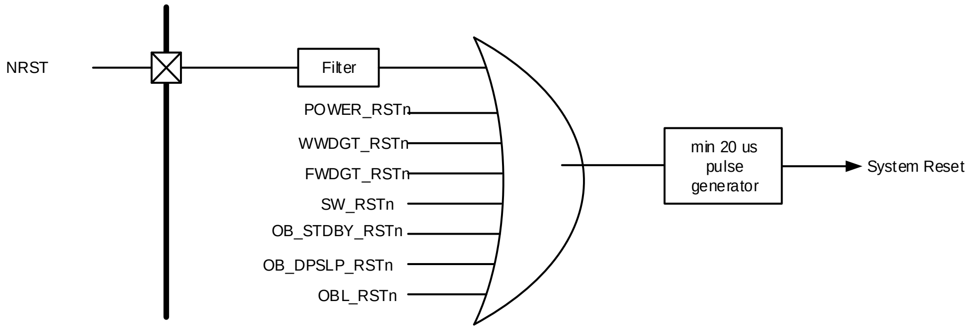
In addition, the MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-4. RCU_RSTSCK Register



MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs.   To prevent a false trigger reset, the NRST pin is recommended to place a capacitor (typically 100nF).

Figure 2-5. System Reset Circuit

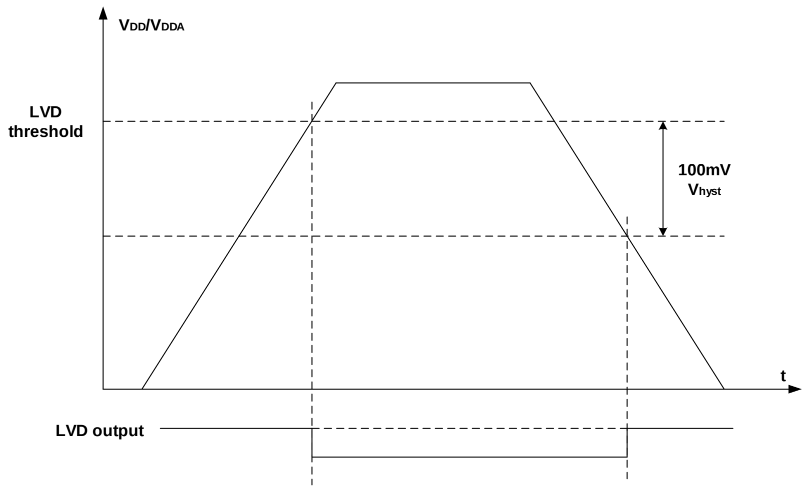


2.2.1. LVD

The function of LVD is to detect whether the V_{DD}/V_{DDA} supply voltage is lower than the low voltage detection threshold, which is configured by the LVDT[2:0] bits in the power control register (PMU_CTL). LVD is enabled by setting the LVDEN bit. The LVDF bit located in the power status register (PMU_CS) indicates whether V_{DD}/V_{DDA} is higher or lower than the LVD threshold voltage event. This event is connected to the 16th line of EXTI. The user can configure EXTI by Line 16 generates a corresponding interrupt. ***Figure 2-6. LVD Threshold Waveform*** shows the relationship between the V_{DD}/V_{DDA} supply voltage and the LVD output signal. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The value of the hysteresis voltage V_{hyst} is 100mV.

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

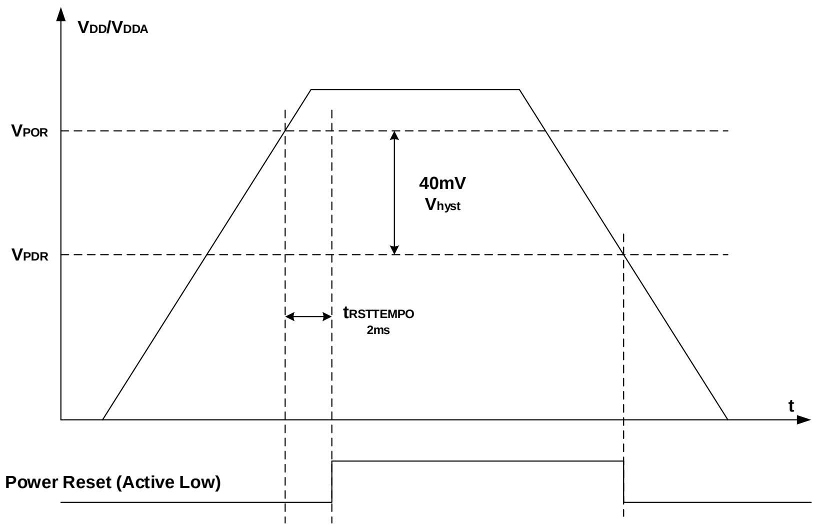
Figure 2-6. LVD Threshold Waveform



2.2.2. POR / PDR

The chip integrates a POR/PDR (power-on/power-down reset) circuit to detect V_{DD}/V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. V_{POR} is the threshold voltage of power-on reset, and the typical value is about 1.71 V, and V_{PDR} is the threshold voltage of power-down reset, and the typical value is about 1.67 V. The value of the hysteresis voltage V_{hyst} is about 40mV.

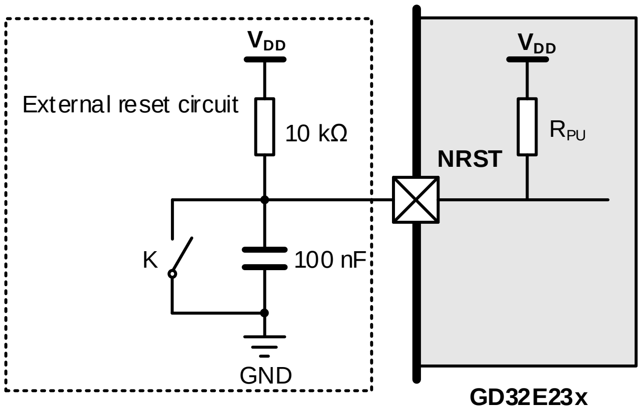
Figure 2-7. Power-on/power-down reset waveforms



2.2.3. NRST Pin

For the NRST pin of the MCU, it is recommended to place a capacitor (typically 100 nF) in the NRST pins to prevent a false trigger reset.

Figure 2-8. Recommend External Reset Circuit

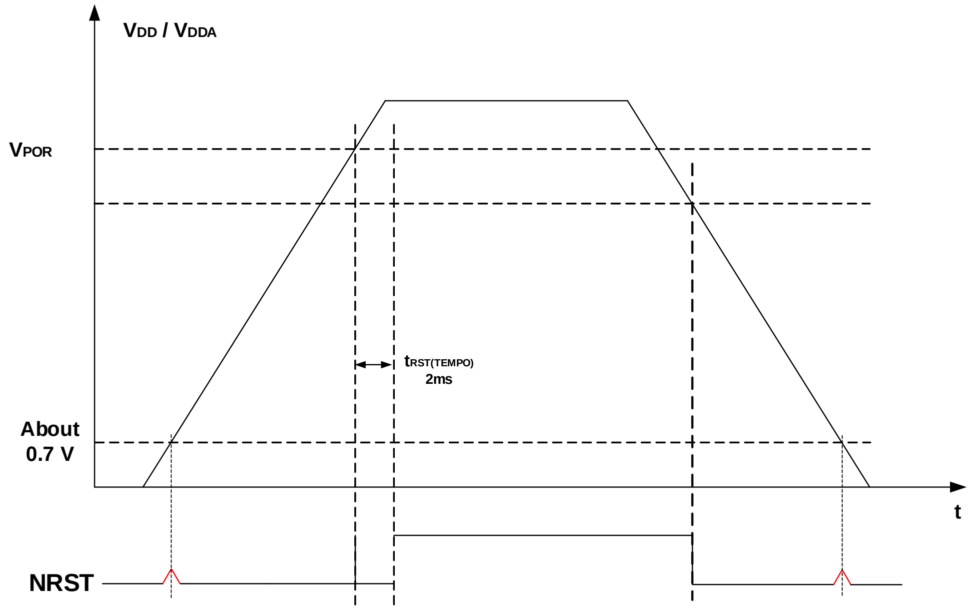


Note:

1. The internal pull-up resistor R_{PU} is 40kΩ, the pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.
5. The internal pull-up resistor R_{PU} = 40kΩ, it is recommended to connect an external pull-up resistor of 10kΩ, so that the voltage interference will not cause the chip to work abnormally.

Due to the threshold voltage characteristics of MOS transistors, during the power-up and power-down process of the chip, when V_{DD} / V_{DDA} is less than 0.7V, the internal pull-down MOS transistor of the chip will not pull the NRST pin low. In other words, during the power-up and power-down process, when V_{DD} / V_{DDA} is approximately 0.7V, a small pulse may occur, which does not affect the normal operation of the chip. This is illustrated by the red pulse shown in ***Figure 2-9. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram***.

Figure 2-9. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram



Due to the difference in charging and discharging speeds, the duration of the pulse on the falling edge is slightly longer than on the rising edge, with both durations being in the millisecond range.

2.3. Clock

GD32F4xx series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4-32 MHz external high-speed crystal oscillator (HXTAL)
- Internal 8 MHz RC oscillator (IRC8M)
- Internal 28 MHz RC oscillator (IRC28M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 40 kHz RC oscillator (IRC40K)
- PLL clock source can be selected from HXTAL or IRC8M
- HXTAL clock monitor

Figure 2-10. Clock tree of GD32E230xx / GD32E235xx

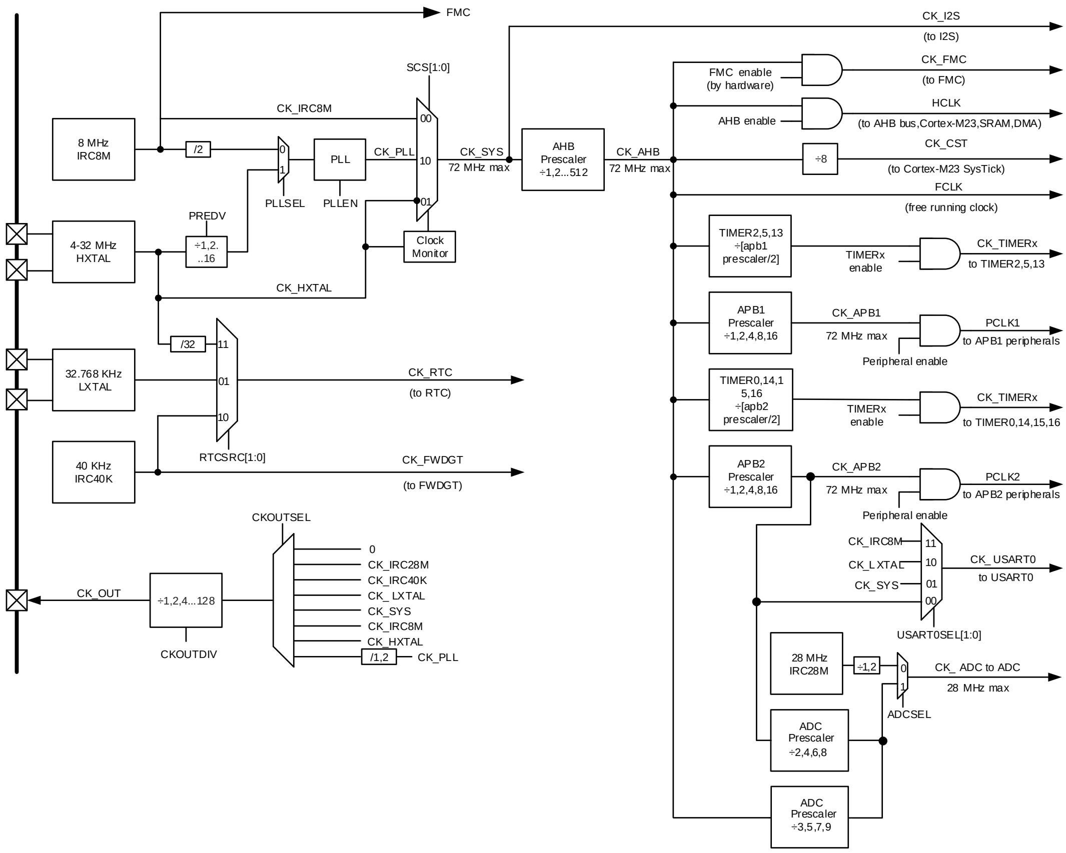
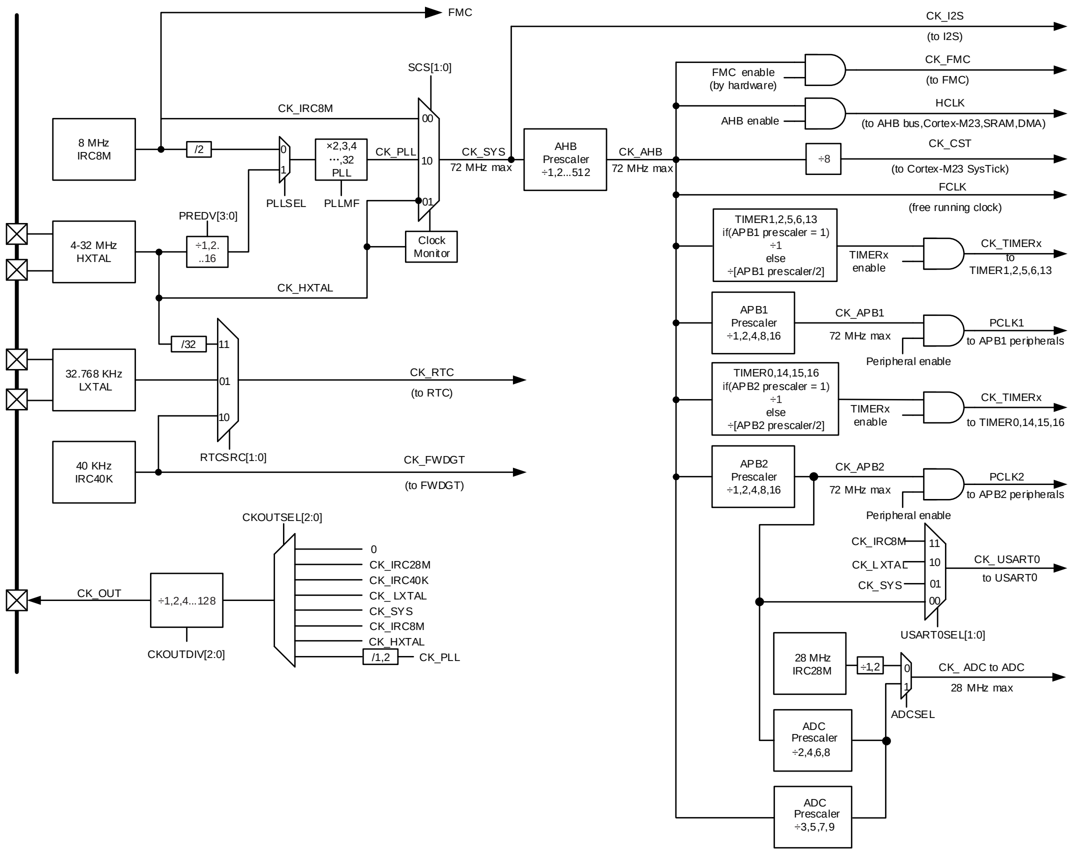


Figure 2-11. Clock tree of GD32E232xx



2.3.1. External high-speed crystal oscillator clock (HXTAL)

4-32MHz external high-speed crystal oscillator (passive crystal) can provide accurate main clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-12. HXTAL External Crystal Circuit

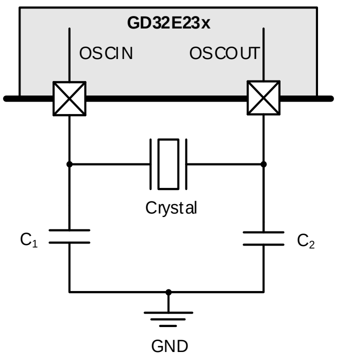
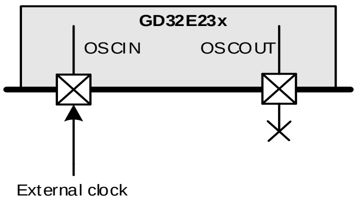


Figure 2-13. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC8M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.
7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSC_OUT and OSC_IN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768KHz low-speed external crystal (passive crystal), which can provide a low-power and high-precision clock source for RTC (packages below 48 pins do not have LXTAL pins). The RTC module of the MCU is equivalent to a counter. The accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-14. LXTAL External Crystal Circuit

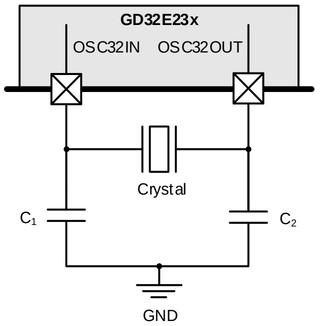
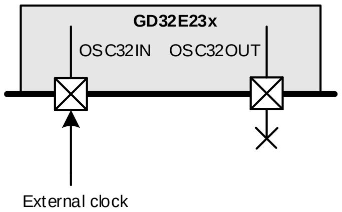


Figure 2-15. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. The MCU can set the drive capability of LXTAL. If it is found that the external low-speed crystal is difficult to vibrate during the actual debugging process, you can try to adjust the drive capability of LXTAL to high drive capability.
4. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the two crystal pins of the MCU due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.3. Clock Output Capability (CKOUT)

GD32E23x series MCUs can output clocks from 32kHz to 72MHz. Different clock signal outputs can be selected by configuring the CKOUT0SEL[2:0] bits of the clock register RCU_CFG0. The corresponding GPIO pins PA8/PA9 need to be configured as multiplexing functions to output selected signal.

Table 2-1. CKOUT0SEL[1:0] Control Bits

CKOUTSEL[2:0]	Clock Source
000	No Clock
001	CK_IRC28M
010	CK_IRC40K
011	CK_LXTAL
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLL or CK_PLL/2

2.3.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL, HXTAL can enable the clock monitoring function. This function must be enabled after the HXTAL start-up delay has elapsed and disabled after the HXTAL has been stopped. Once the HXTAL fault is detected, the HXTAL will be automatically disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to '1' to generate an HXTAL fault event. The interrupt caused by this fault is connected to the non-maskable interrupt NMI of the Cortex®-M23.

Note: If HXTAL is selected as the system or PLL clock source, HXTAL failure will cause the IRC8M to be selected as the system clock source and the PLL will be automatically disabled. The clock source of the RTC needs to be reconfigured.

2.4. Startup Configuration

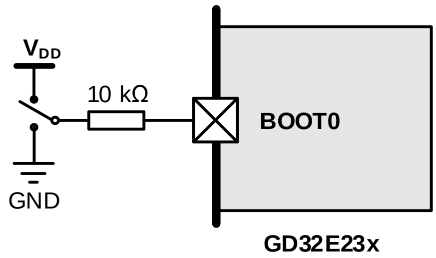
The GD32E23x series provides three startup methods, which can be selected by the user option byte BOOT1_n bit and BOOT0 pin to determine the startup option. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND; when running the System Memory to update the program, the BOOT0 pin needs to be connected high, and the option byte OB_USER[4] keeps BOOT1_n at 1 (this When the corresponding BOOT1 bit is 0), after the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging state.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In GD32E230xx devices, the Bootloader can interact with the outside world through USART0 (PA9 and PA10) or USART1 (PA14 and PA15 or PA2 and PA3). In the GD32E232xx device, the Bootloader can interact with the outside world through I2C0 (PB6 and PB7 for GD32E232Kx or PA9 and PA10 for GD32E232Ex).

Table 2-2. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-16. Recommend BOOT Circuit Design



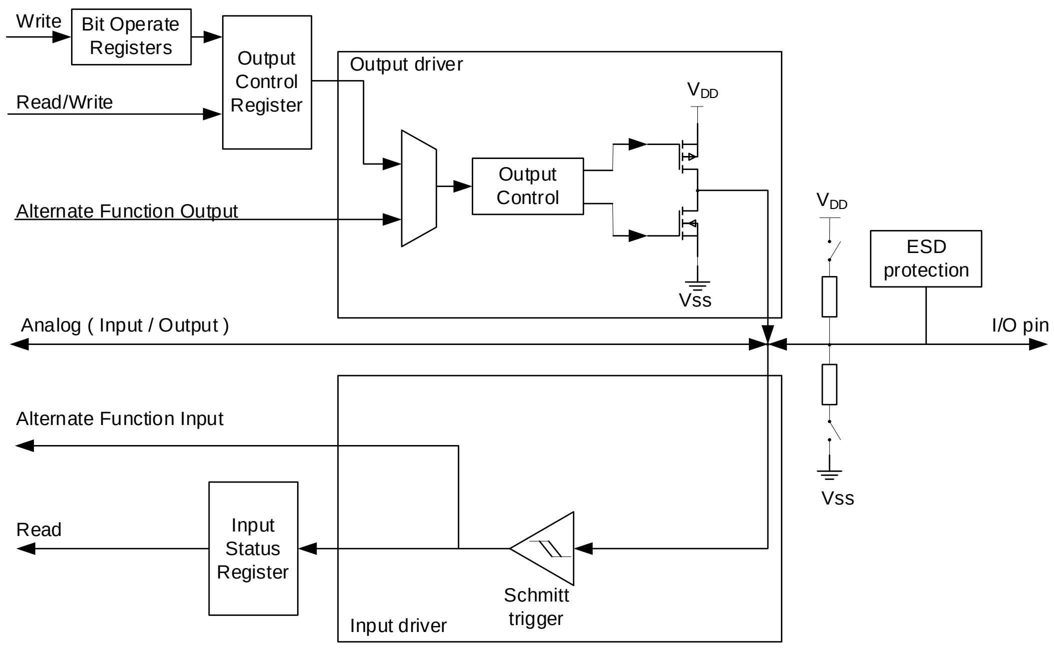
Note: After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset. MCU.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

GD32E230xx can support up to 39 general purpose I/O pins (GPIO), which are PA0 ~ PA15, PB0 ~ PB15, PC13 ~ PC15, PF0 ~ PF1, PF6 ~ PF7; GD32E232xx can support up to 28 general-purpose I/O pins (GPIO), which are PA0 ~ PA15, PB0~PB9, PF0~PF1. Each pin can be independently configured through registers. The basic structure of the GPIO port is shown in the following figure:

Figure 2-17. Basic structure of standard IO



Note:

1. The IO port is divided into 5V tolerance and non-5V tolerance. When using, pay attention to distinguish the voltage tolerance of the IO port, see Datasheet for details.
2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
5. The three IO ports of PC13, PC14, and PC15 have weak drive capability and limited output current capability (about 3mA). When configured in output mode, their operating speed cannot exceed 2MHz (maximum load is 30pF).
6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
7. Non-5V tolerant IO, when the external voltage exceeds V_{DD}, a sink current may be generated.

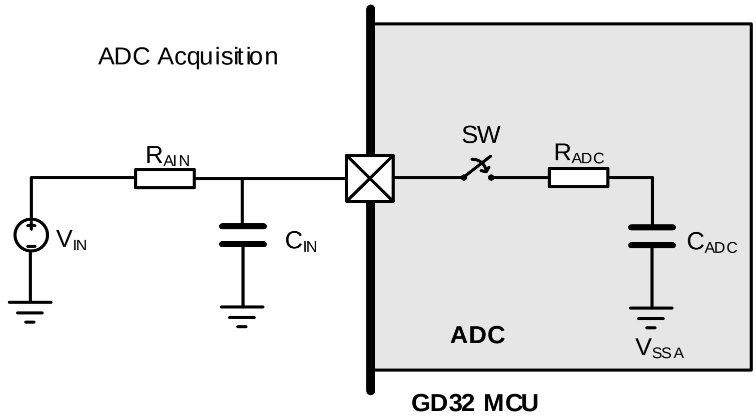
2.5.2. ADC Circuit

The GD32E23x integrates a 12-bit SAR ADC, GD32E230xx has up to 12 channels, can measure 10 external and 2 internal signal sources; GD32E232x has up to 18 channels, can measure 16 external and 2 internal signal sources signal source. The internal signals are the temperature sensor channel (ADC0_CH16) and the internal reference voltage input channel (ADC0_CH17). The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC and is internally connected to ADC0_IN17.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF.

Figure 2-18. ADC Acquisition Circuit Design



When f_{ADC} = 28MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

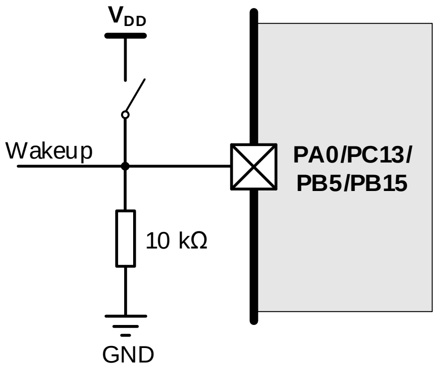
Table 2-3. f_{ADC} =28MHz Relationship between sampling period and external input impedance

T_S (cycles)	t_S (us)	$R_{AIN\ max}$ (kΩ)
1.5	0.05	0.88
7.5	0.27	6.40
13.5	0.48	11.92
28.5	1.02	25.72
41.5	1.48	37.68
55.5	1.98	50.56
71.5	2.55	65.29
239.5	8.55	219.86

2.5.3. Standby mode wake-up circuit

The GD32E23x series supports three low-power modes, namely sleep mode, deep-sleep mode and standby mode. The standby mode with the lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. There are a total of 4 WKUP pins. At this time, there is no need to configure the corresponding GPIO, just configure the WUPENx bit in the PMU_CS register. The reference circuit design corresponding to the WKUP wake-up pin is as follows:

Figure 2-19. Recommend Standby external wake-up pin circuit design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.6. Download the debug circuit

The GD32E23x series cores only support SWD debug interface, not JTAG interface. The SWD interface standard is a 5-pin interface, of which 2 are signal interfaces.

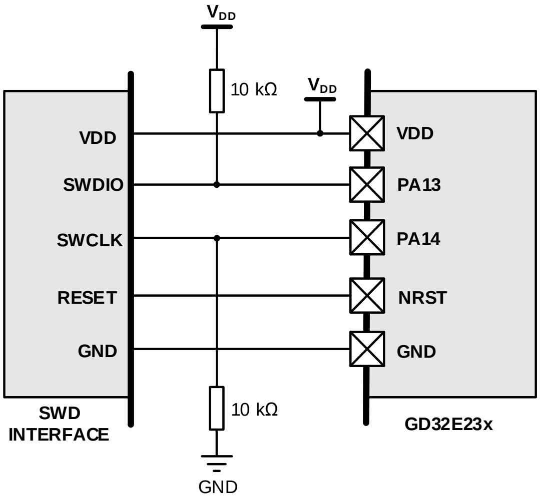
Note: After reset, the debug related ports are in input PU/PD mode, where:

PA13：SWDIO is in pull-up mode.
PA14：SWCLK is in pull-down mode.

Table 2-4. SWD Download Debug Interface Assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-20. Recommend SWD Wiring Reference Design



There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1kΩ resistor.

2.7. Reference Schematic Design

Figure 2-21. GD32E230xx / GD32E235xx Recommend Reference Schematic Design

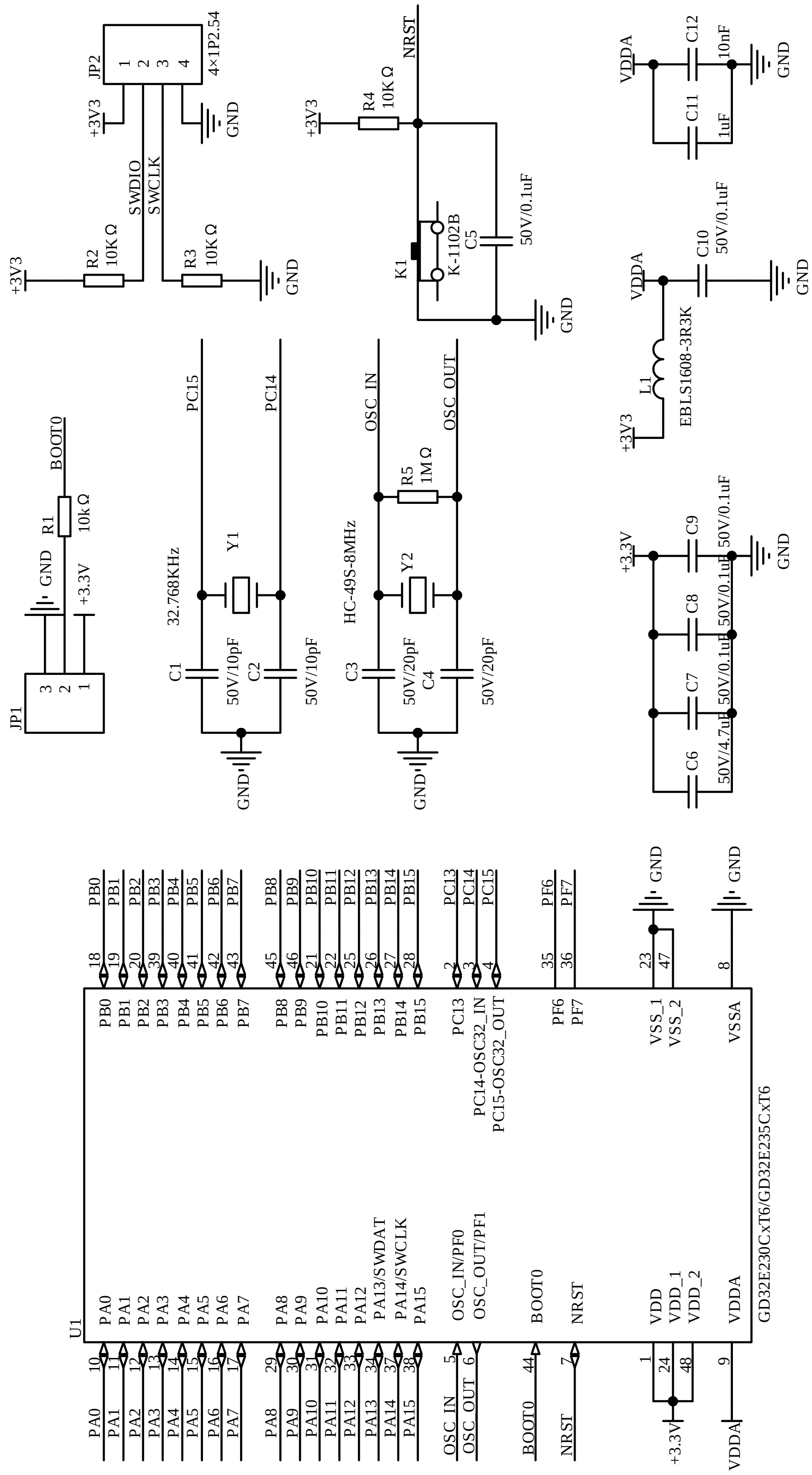
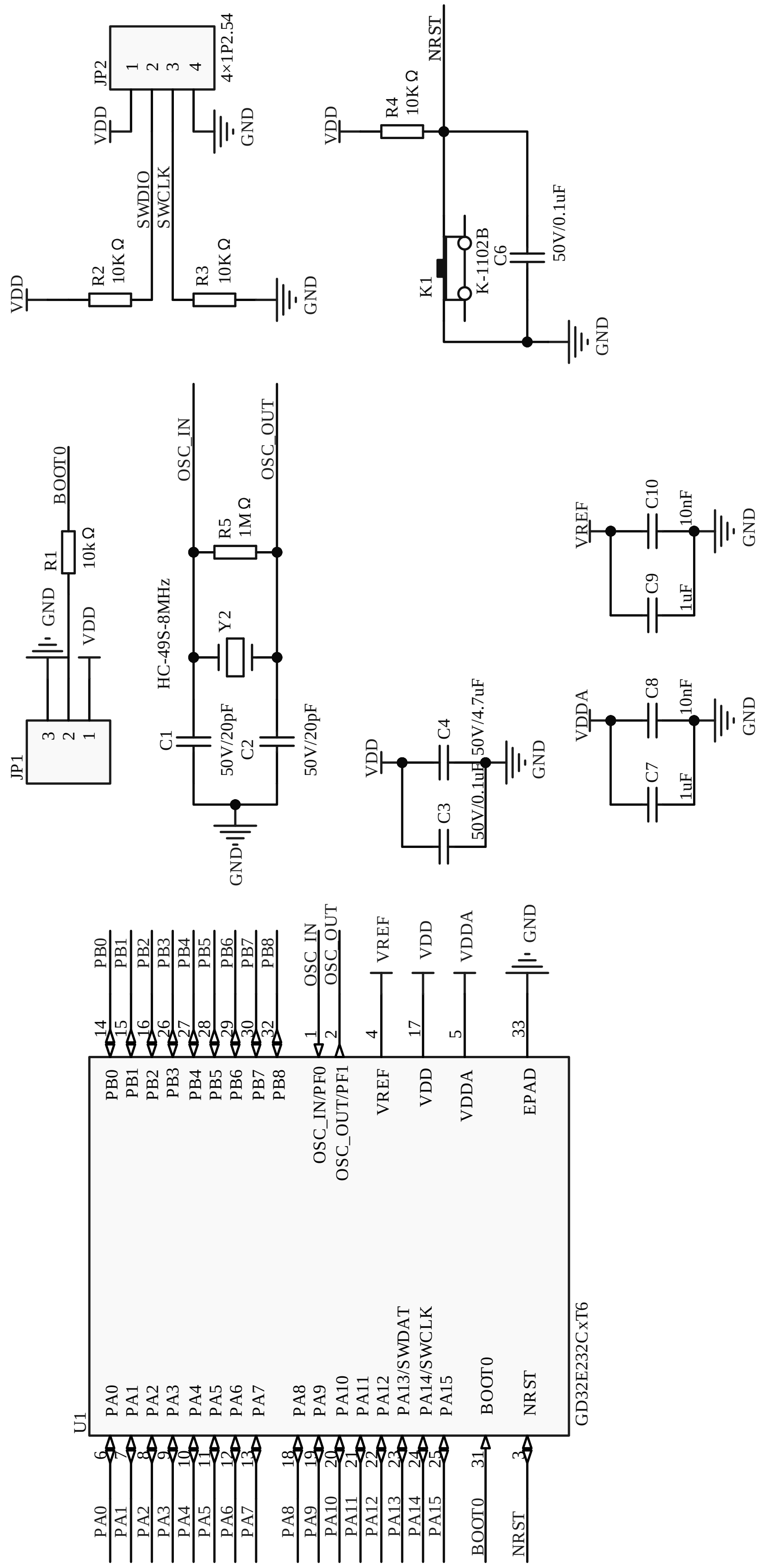


Figure 2-22. GD32E232xx Recommend Reference Schematic Design



3. PCB Layout Design

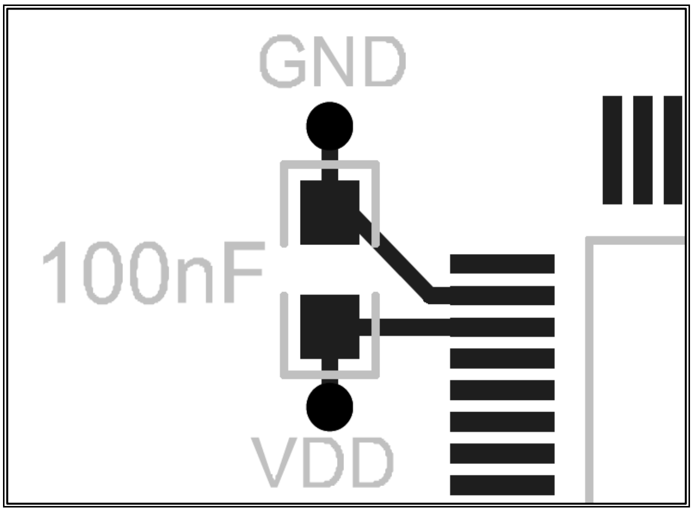
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32E23x series power supply has three power supply pins: V_{DD}, V_{DDA} and V_{BAT}. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

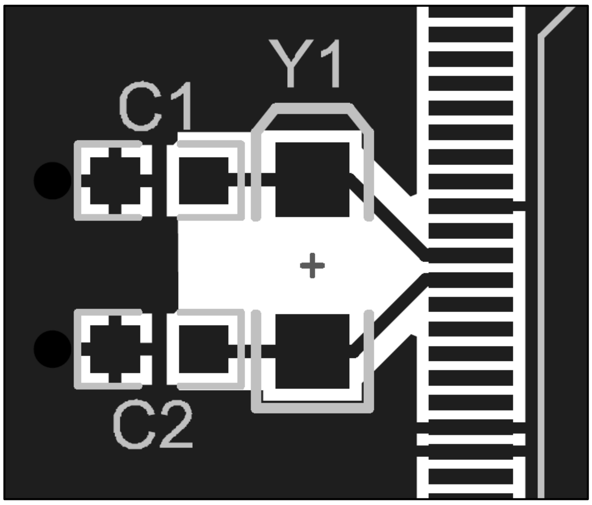
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32E23x series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



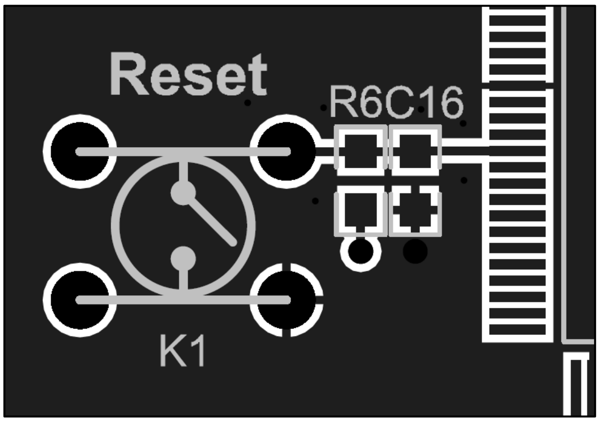
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

4. Package Description

The GD32E230xx series has a total of 7 package types, namely TSSOP20, LGA20, QFN28, QFN32, QFN48, LQFP32 and LQFP48.

The GD32E232xx series has two packages, QFN24 and QFN32 (4x4).

The GD32E235xx series has a total of 7 package types, namely TSSOP20, LGA20, QFN28, QFN32, QFN48, LQFP32 and LQFP48.

Table 4-1. Package Description

Ordering code	Package
GD32E230FxPx	TSSOP20(6.5x4.4, 0.65 pitch)
GD32E230ExPx	TSSOP24(7.8x6.4,0.65 pitch)
GD32E230FxV6	LGA20(3x3, 0.5 pitch)
GD32E230GxUx	QFN28(4x4, 0.4 pitch)
GD32E230KxUx	QFN32(5x5, 0.5 pitch)
GD32E230CxU6	QFN48(7x7, 0.5 pitch)
GD32E230KxT6	LQFP32(7x7, 0.8 pitch)
GD32E230CxTx	LQFP48(7x7, 0.5 pitch)
GD32E232ExU7	QFN24(3x3, 0.4 pitch)
GD32E232KxQ7	QFN32(4x4, 0.4 pitch)
GD32E235FxP6	TSSOP20(6.5x4.4, 0.65 pitch)
GD32E235FxV6	LGA20(3x3, 0.5 pitch)
GD32E235GxU6	QFN28(4x4, 0.4 pitch)
GD32E235KxU6	QFN32(5x5, 0.5 pitch)
GD32E235CxO6	QFN48(7x7, 0.5 pitch)
GD32E235KxT6	LQFP32(7x7, 0.8 pitch)
GD32E235CxTx	LQFP48(7x7, 0.5 pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Sep.23, 2022
1.1	1. Update section 2.1.4 to provide all package power supply design diagrams showing how the relevant pins are connected inside the chip 2. Update 2.7 Design the power decoupling capacitor combination by referring to the schematic diagram	Jun.21, 2023
1.2	1. Add information about GD32E230CxU6 QFN48 2. Add information about GD32E235xx	Apr.18, 2024
1.3	1. Refine the content related to power supply detection and reset, and add Section 2.2	Dec.15, 2024

Important Notice